Enhancing RTL Power Accuracy with Advanced Buffer Modeling for Improved Efficiency and Correlation

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Motivation: Improve RTL Power Accuracy

Problem statement:

- At RTL level, buffers inserted at place and route stage are often not accounted for power analysis.
- These buffers impact switching activity, drive strength, and load – yet ignored at RTL, leads to a significant mismatch between RTL and netlist power.

Design impact:

- Inaccurate power budgets and misinformed design decisions.
- Ineffective RTL power optimizations due to wrong hotspot targeting.

Our goal:

Accurately modeling buffer behavior at the RTL level helps narrow the power estimation gap with the netlist, enabling earlier, more informed design decisions and greater confidence in power budgeting.

Background: Inferior RTL Power Accuracy due to Complex Buffer Structures

Challenges faced during the correlation:

- Combinational and buffer power accuracy at RTL stage is essential to achieve good correlation with sign-off power.
- Highly complex backend implementations in advanced tech node, such as high fanout buffer tree, repeater, etc., make the RTL correlation challenging.
- There is growing need for a seamless solution to improve combinational logic & buffer power accuracy at RTL stage. Buffers contribute as much as 10%-15% of total design power.

Requirement:

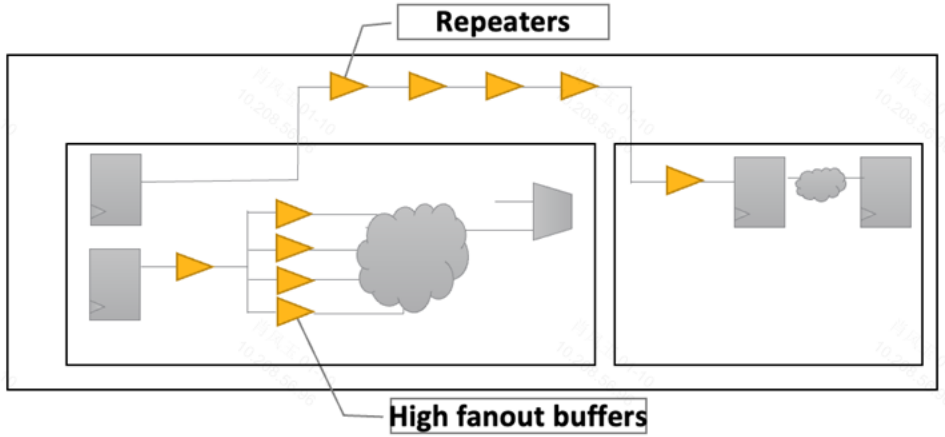
- Need advanced methodology to model buffer at RTL stage.

Component	Correlation
Register	Good
Clock	Good
Memory	Good
Combinational	Bad
Buffer	Extremely bad

Area of focus in this proposal

Main Idea: Introduce Advanced Buffer Modeling (ABM)

- PowerArtist RTL power analysis has enhanced the PowerArtist Calibration and Estimation (PACE) model, by including high fanout net buffer tree synthesis, repeater, reset, scan-enable and spare cells insertion.
- The PACE buffer and repeater models capture statistical high fanout net buffer trees and repeater chains from the Gate netlist and used for RTL power analysis.



- Buffer trees for high fanout nets
- Repeater chains for module crossing depth

Methodology: Enabling Advanced Buffer Modeling

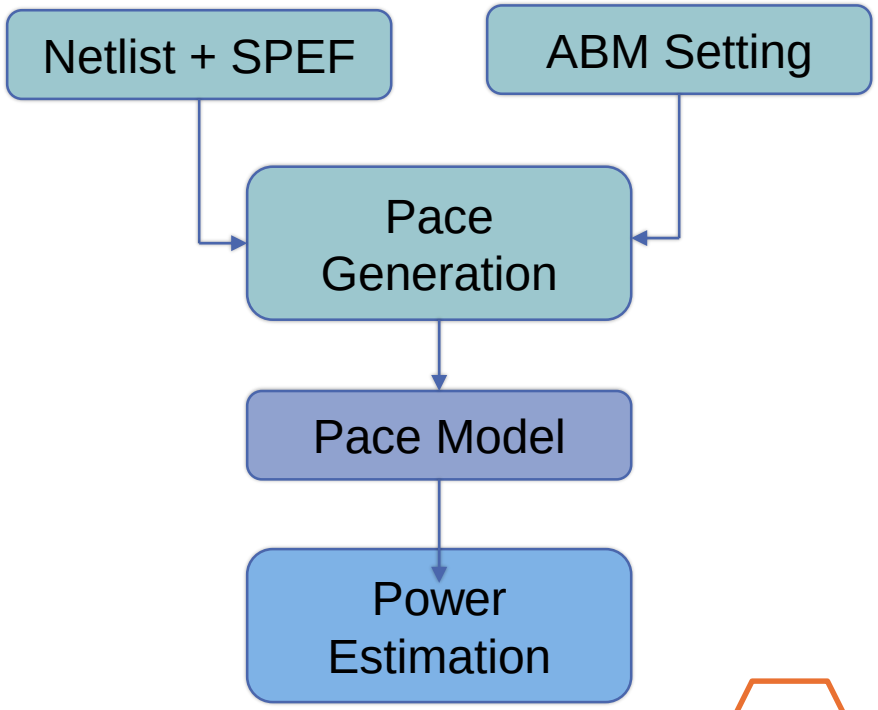
Advanced buffer model flow can be enabled by a two-step approach for improved RTL power correlation with Gate netlist.

Two steps flow to model buffer power:

- Step 1: generate pace model with buffer modeling.
  - Add key words to specify backend cells to help EDA tools to identify such structure better.

clock_cells	hold_buffer_cells	decap_cells
antenna_cells	filler_cells	welltap_cells
level_shifter_cells	isolation_cells	always_on_cells
switch_cells	reset_instance	hold_buffer_instance

- Step 2: use pace model with buffer modeling to estimate power.



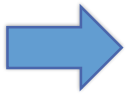
Methodology: Advanced Buffer Modeling Settings

- **To enable ABM**:

```
pa_set generate_pace_model_category {buffertree repeater cap cell clock}
pa_set use_pace_model_category {buffertree repeater cap cell clock}
```

- Specify the naming regex of **power management cells** and **physical cells** used in the gate netlist

```
pa_set pace_clock_cells { CK* }
pa_set pace_clock_isolation_cells { CKLI* }
pa_set pace_clock_level_shifter_cells { CKLV* }
pa_set pace_level_shifter_cells { LVL* }
pa_set pace_isolation_cells { IS* }
pa_set pace_antenna_cells { ANTENNA* }
pa_set pace_filler_cells { *FILL* }
pa_set pace_welltap_cells { TAPCELL* }
pa_set pace_always_on_cells { PT* }
pa_set pace_hold_buffer_cells { DEL* }
pa_set pace_switch_cells { HDR* }
pa_set pace_decap_cells { GDCAP* }
```



Snippet of PACE report with buffer categorization:

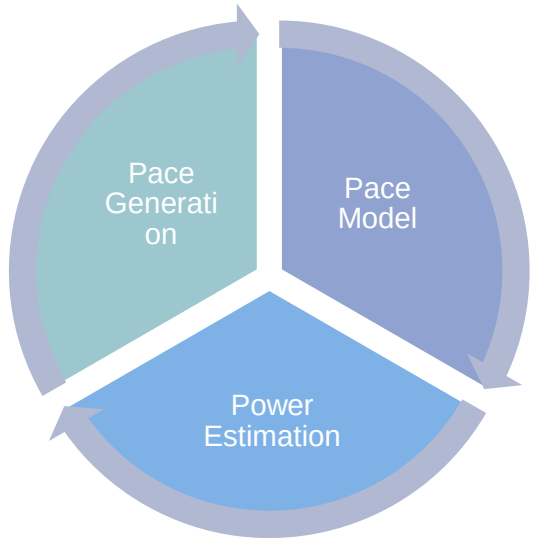
```
Buffer cells:
-------------------------------------------------------------------------------
  Function: always_on
      Cell: BUFAONX1MTL            lvt                          LOW_VT
      Cell: BUFAONX2MTH            hvt                          HIGH_VT
  Function: buffertree
      Cell: BUFX1MTH               hvt                          HIGH_VT
  Function: hold
      Cell: DELX1MTH               hvt                          HIGH_VT
  Function: pad
      Cell: INVPADSFX1MTH          hvt                          HIGH_VT
  Function: repeater
      Cell: INVX2MTH               hvt                          HIGH_VT
      Cell: INVX4MTL               lvt                          LOW_VT


Physical/Power management cells
-------------------------------------------------------------------------------
  Function: antenna
      Cell: ANTENNA1MTL            lvt                          LOW_VT
      Cell: ANTENNA2MTH            hvt                          HIGH_VT
  Function: decap
      Cell: DCAP2MTH               hvt                          HIGH_VT
      Cell: DCAP4MTL               lvt                          LOW_VT
  Function: filler
      Cell: FILL1MTH               hvt                          HIGH_VT
  Function: power_switch
      Cell: HDRBUFX1MTH            hvt                          HIGH_VT
  Function: well_tap
      Cell: TAPCELL1MTH            hvt                          HIGH_VT
```

Value: Make Power More Predictable and Accurate at RTL Stage

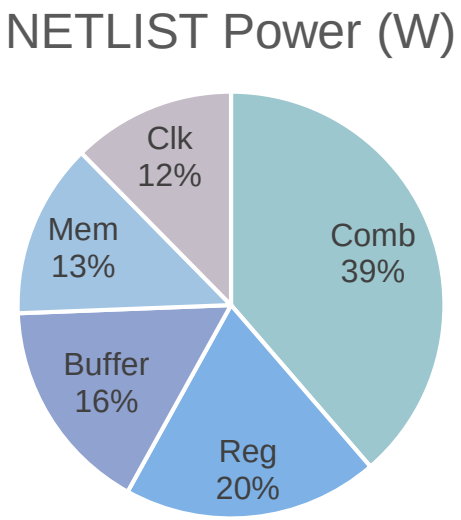
- This technology not only impacts combinational and buffer power, it also impacts register and memory power. So it makes RTL power more predictable and accurate. Of course, the improvements in combinational and buffer logic are more significant.
- Correlation is not just about comparing power differences between RTL and the netlist; the key objective is to improve the evaluation model to minimize these differences. By ensuring the model's accuracy and reliability, we can further refine the power generation flow to produce a precise model, ultimately achieving more accurate power estimations early in design cycle.

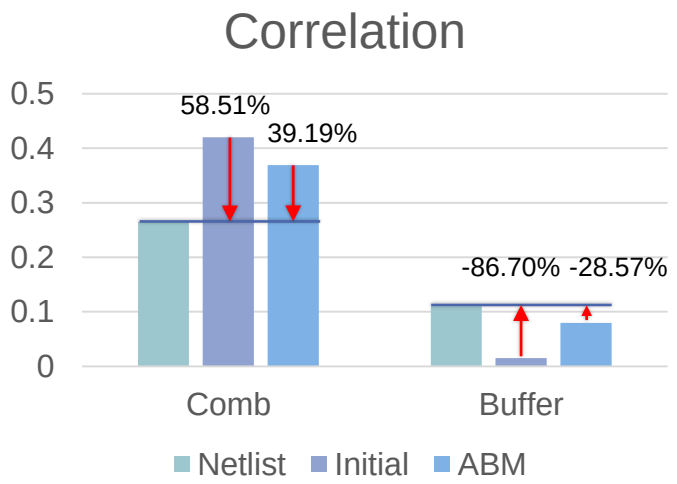
Component	Impact
Register	Yes
Clock	No
Memory	Yes
Combinational	Yes
Buffer	Yes



Evidence 1: Better Correlation for Combinational and Buffer Logic

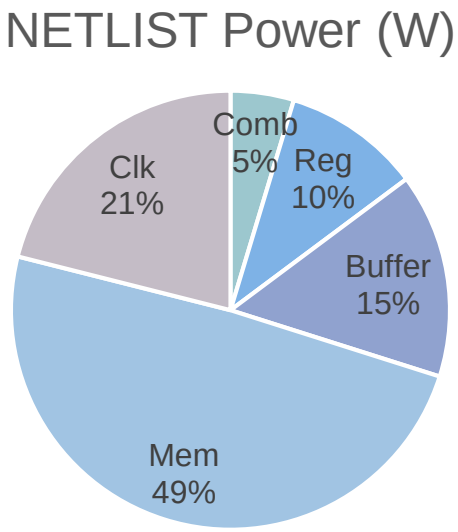
In design A, the power correlation for buffer category has been improved from **-86.70% to -28.57%** by enabling ABM. This results in an improved combinational logic power correlation from **58.51% to 39.19%**. The introduction of advanced buffer modelling has helped to bridge the overall power correlation gap between netlist and RTL by proper modelling of buffers.

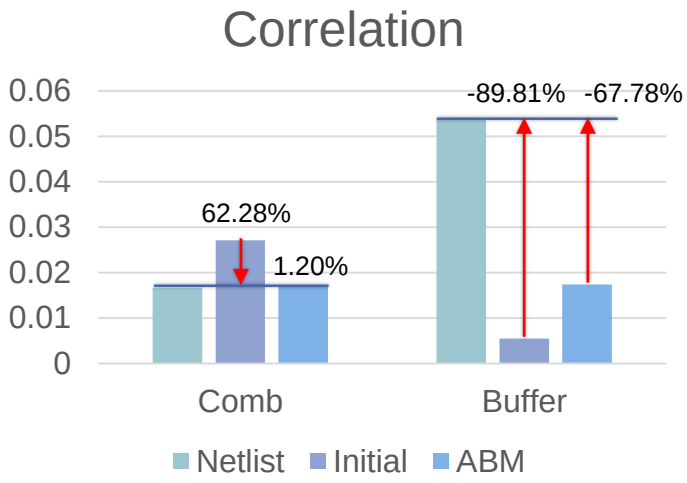




Evidence 2: Better Correlation for Combinational and Buffer Logic

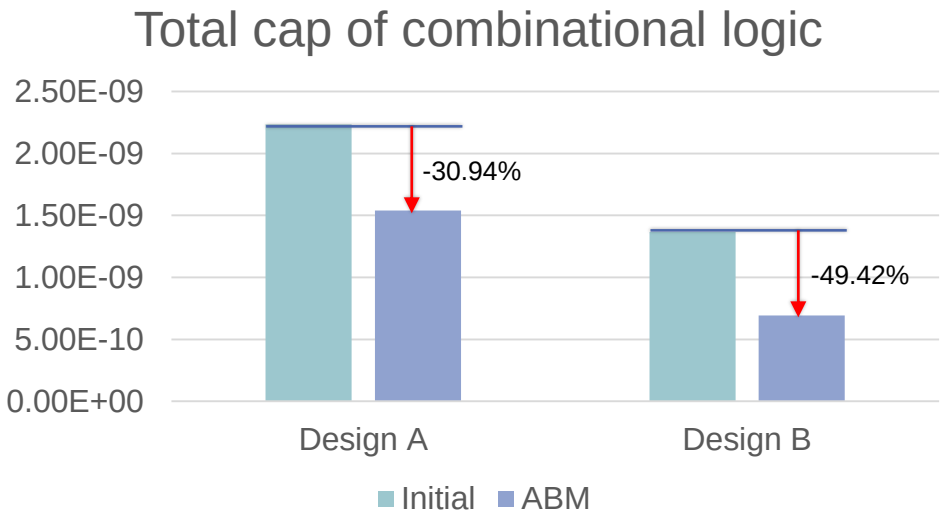
In design B, the correlation trend is similar to design A, with the buffer category power correlation improving from **-89.81% to -67.78%**. In addition, the correlation of combinational logic category has been improved from **62.28% to 1.20%**. The difference for buffer logic under advanced buffer modeling is caused by specific layout.

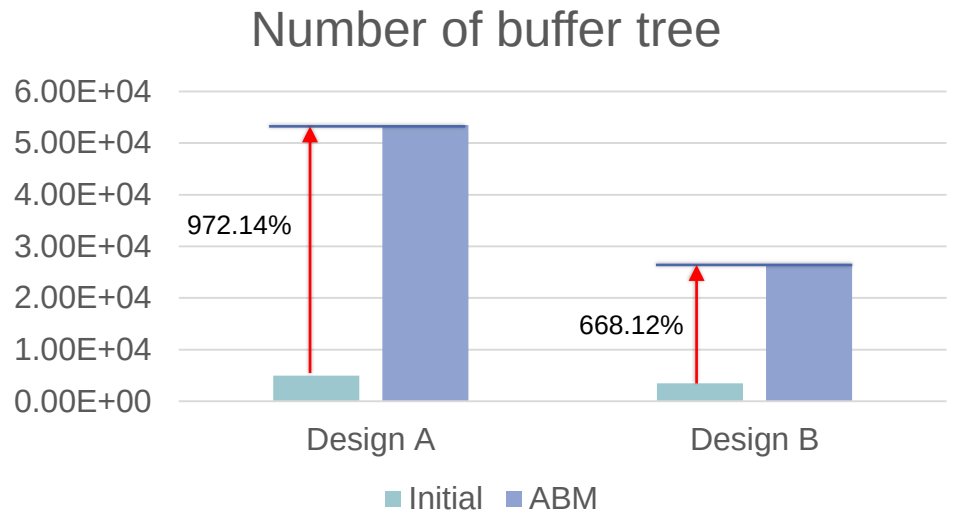




Evidence: Influence of ABM on Combinational and Buffer Logic

For combinational logic, after analysis, total cap is decreased **30.94%** for design A and total cap is decreased **49.42%** for design B.
For buffer logic, after analysis, number of buffer tree is increased **972.14%** for design A and number of buffer tree is increased **668.12%** for design B.





Summary: Conclusion

- For current designs, buffers inserted at place and route stage contribute more and more power, it makes hard to correlate RTL and NETLIST power.
- To solve this issue, we introduced the advanced buffer modeling methodology at RTL stage, this methodology captures statistical high fanout net buffer trees and repeater chains from the gate netlist and used for RTL power analysis.
- By using this methodology, we got better correlation between RTL and NETLIST.

Design	Component	Initial (%)	ABM (%)
A	Buffer	-86.70	-28.57
	Combinational	58.51	39.19
B	Buffer	-89.81	-67.78
	Combinational	62.28	1.20